

Lab 2: Cadence Tutorial on Layout and DRC/LVS/PEX

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This document contains all of the electrical properties of the devices in the process. It also contains layout design rules and other information about the process. You can find a cross section of the process on page 28.

Introduction

This tutorial describes how to generate a layout view in the Cadence Virtuoso Layout Editor, how to perform layout verification in Calibre, and how to re-simulate your design with extracted parameters in Spectre. In the first section, you will generate a layout for a simple CMOS inverter. In the second, you will create a buffer using the inverter cell you have created.

When doing layout, a techfile must be attached to the library. This defines layers, parameterized cells (pcells) and other layout-related technology information. This should have been set in Lab 1, but we will double check the techfile. To do this, start virtuoso in your cadence directory.

```
% cd -/www413/  
% module load /afs/umich.edu/class/ece/modules/ece413/15  
% virtuoso &
```

Open the Library Manager from the CTW by browsing to

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Cadence Lab Manual

Tobias Bleicker



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